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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,428	01/06/2004	Lynn Patterson	DY-03	3799

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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/752,428	PATTERSON ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 29th of March 2006. Claims 1 and 2 have been amended; no claim has been canceled; and claims 3-14 have been newly added since the Non-Final Office Action was mailed on 27th of September 2005. Currently, claims 1-14 are pending in this Application.

Specification

2. The disclosure is objected to because of the following informalities:

Substitute "buss" in lines 18 and 20 on page 1, and in line 5 on page 2, by --bus--.

Substitute "A interconnected" in line 20 on page 5 by --An interconnected--.

Appropriate correction is required.

Claim Objections

3. Claims 1, 2, 4, 6, 8, and 12 are objected to because of the following informalities:

In the claim 6, delete "A system 1. (Currently Amended)" in line 1.

The claim 1 recites the subject matter "the network" in line 8. However, it has not been specifically clarified in the claim 1. Therefore, the Examiner presumes that the term "the network" could be considered as --a network-- in light of the specification since it is not defined in the claim.

The claim 2 recites the subject matter "the circuit card data bus" in lines 8-9. However, it has not been specifically clarified in the claim 2. Therefore, the Examiner presumes that the term "the circuit card data bus" could be considered as --a circuit card data bus-- in light of the specification since it is not defined in the claim.

The claims 4, 8, and 12 respectively recite the subject matter "the terminating point" in lines 1-2. However, it has not been specifically clarified in the respective claims 4, 8, and 12, and their respective intervening claims. Therefore, the Examiner presumes that the term "the terminating point" could be considered as --a terminating point-- in light of the specification since it is not defined in the claims, respectively.

The claim 14 recites the subject matter "the data" in line 2. However, it has not been specifically clarified in the claim 14 and its intervening claims. Therefore, the Examiner presumes that the term "the data" could be considered as --data-- in light of the specification since it is not defined in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 8 recites the claimed subject matter "bridge" in line 1. However, its parent claim 6 recites two different subject matters "bridge" in lines 4 and 6, respectively. Therefore, it fails to clearly point out which one of the two different subject matters "bridge" in lines 4 and 6 of the claim 6 is the antecedent basis of the recited subject matter "bridge" in the claim 8, and then it makes the claim 8 be indefinite.

The Examiner presumes that the term "bridge" in line 6 of the claim 6 could be considered as --the bridge-- in light of the specification since it is not clearly pointed out in the claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 5-7, and 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan [US 6,950,893 B2].

Referring to claim 1, Chan discloses a PCI-based mezzanine card (PMC; i.e., Hybrid Switching Module 400 in Fig. 4), comprising:

- a data bus connector (i.e., PCI CPU bus connection 402 and PCI main bus connection 404 in Fig. 4) for connecting the PCI-based mezzanine card (PMC) to a data bus (i.e., PCI backplane busses 508, 510, 512, and 514 in Fig. 5) of a circuit card (i.e., I/O Chassis 528 of Fig. 5);
- a switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) comprising a network port (i.e., port for I/O Links 406 in Fig. 4) that allows the switch (i.e., said Crossbar Switch & Arbiter) to connect directly to a second switch (e.g., HSM 500 being directly connected to HSM 502 in Fig. 5) on a network (i.e., I/O Links 112 in Fig. 1; See col. 5, lines 52-55); and
- a bridge (i.e., Bridge 410 of Fig. 4) connected between the switch (i.e., said Crossbar Switch & Arbiter) and the data bus connector (i.e., said PCI CPU bus and main bus

connection; actually, said Bridge connected between said Crossbar Switch & Arbiter and said PCI main bus connection; See col. 5, lines 41-45).

Referring to claim 2, Chan discloses a system (i.e., computer system 100 in Fig. 1) for networking computer cards (i.e., connecting single board computers 102, 116 in Fig. 1) for data transfer (See col. 3, lines 31-48), comprising:

- a plurality of networked circuit cards (i.e., a plurality of single board computer/hybrid switching module pairs 500, 502, 504, and 506 in Fig. 5), each card (e.g., single board computer/hybrid switching module pair 500 of Fig. 5) comprising:
    - a processor (i.e., CPU in Fig. 5) connected to a bus (i.e., PCI CPU bus connection 402 of Fig. 4);
    - a PCI-based mezzanine card (PMC; i.e., Hybrid Switching Module 400 in Fig. 4), connected to the circuit card (e.g., HSM A 104 coupled to System Host SBC A 102 in Fig. 1) and connected to the bus (i.e., said HSM 400 connected to said PCI CPU bus connection 402 in Fig. 4) for access to the processor of the circuit card (See col. 5, lines 46-48), comprising
        - a switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) connected to a network (i.e., I/O Links 112 in Fig. 1; See col. 5, lines 52-55) and
        - a bridge (i.e., Bridge 410 of Fig. 4) that is connected between the switch (i.e., said Crossbar Switch & Arbiter) and a circuit card data bus (i.e., PCI main bus connection 404 of Fig. 4; See col. 5, lines 41-45)
    - wherein each switch (e.g., Crossbar Switch & Arbiter in HSM 500 in Fig. 5) is directly connected to at least one other switch over the network (i.e., Crossbar Switch & Arbiters in HSM 502, 504, and 506 in Fig. 5), and

- each PMC bridge (i.e., each Bridge in HSM 500, 502, 504, and 506 in Fig. 5) can bridge data transfer from each processor between each circuit card's data bus (i.e., said PCI main bus connection of the respective HSM 500, 502, 504, and 506 in Fig. 5) and each PMC switch (i.e., respective Crossbar Switch & Arbiters in HSM 500, 502, 504, and 506 in Fig. 5) that is connected to the network (See col. 5, line 66 through col. 6, line 16).

Referring to claim 3, Chan teaches

- when the switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) is directly connected to the second switch (i.e., HSM 500 being directly connected to HSM 502 in Fig. 5) over the network (i.e., I/O Links 112 in Fig. 1; See col. 5, lines 52-55), the PMC (i.e., Hybrid Switching Module 400 of Fig. 4) allows data transfers through the network (i.e., said I/O Links) to and from the bus of the circuit card (i.e., PCI backplane busses 508, 510, 512, and 514 of I/O Chassis 528 in Fig. 5; See col. 5, line 66 through col. 6, line 16).

Referring to claim 6, Chan discloses a device for digital processing (i.e., Hybrid Switching Architecture in Fig. 5), comprising:

- a circuit card (i.e., single board computer/hybrid switching module pair 500 of Fig. 5) comprising a processor (i.e., CPU of said pair 500 in Fig. 5) connected to a data bus (i.e., PCI CPU bus connection 402 and PCI main bus connection 404 in Fig. 4);
- a PCI-based mezzanine card (PMC; i.e., Hybrid Switching Module 400 in Fig. 4), comprising a switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) and a bridge (i.e., Bridge 410 of Fig. 4),

- wherein the switch (i.e., said Crossbar Switch & Arbiter) comprises a network port (i.e., port for I/O Links 406 in Fig. 4) that allows the switch (e.g., said Crossbar Switch & Arbiter in HSM 500 in Fig. 5) to connect directly to other switches (i.e., said Crossbar Switch & Arbiter in HSMs 502, 504, and 524 in Fig. 5) on a network (i.e., I/O Links 112 in Fig. 1; See col. 5, lines 52-55 and col. 6, lines 8-16) and the bridge (i.e., said Bridge) that is connected between the switch (i.e., said Crossbar Switch & Arbiter) and the circuit card data bus (i.e., said PCI CPU bus and main bus connection; actually, said Bridge connected between said Crossbar Switch & Arbiter and said PCI main bus connection; See col. 5, lines 41-45).

Referring to claim 7, Chan teaches

- when the switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) is directly connected to another switch (i.e., HSM 500 being directly connected to HSM 502 in Fig. 5) over the network (i.e., I/O Links 112 in Fig. 1; See col. 5, lines 52-55), the PMC (i.e., Hybrid Switching Module 400 of Fig. 4) allows data transfers through the network (i.e., said I/O Links) to and from the processor of the circuit card (i.e., CPU of single board computer/hybrid switching module pair 500 in Fig. 5; See col. 5, line 66 through col. 6, line 16).

Referring to claims 5 and 9, Chan teaches

- the switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4) comprising a plurality of network ports (i.e., a plurality of ports for I/O Links 516, 518, 520, and 522 in Fig. 5) for connecting the switch (e.g., said Crossbar Switch & Arbiter in HSM 500 in Fig. 5) directly

to a plurality of other switches (i.e., said Crossbar Switch & Arbiter in HSMs 502, 504, and 524 in Fig. 5) on the network (i.e., I/O Links 112 in Fig. 1; See col. 6, lines 8-16).

Referring to claim 10, Chan teaches

- the bus (i.e., PCI CPU bus connection 402 and PCI main bus connection 404 in Fig. 4) is a PCI bus (See col. 5, lines 31-38).

Referring to claim 11, Chan teaches

- the data bus (i.e., PCI main bus connection 404 of Fig. 4) is a PCI bus (See col. 5, lines 31-38).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 4, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan [US 6,950,893 B2] as applied to claims 1-3, 5-7, and 9-11 above, and further in view of Ravinovitz et al. [US 2004/0083324 A1; hereinafter Ravinovitz].

Referring to claims 4, 8, and 12, Chan discloses all the limitations of the claims 4, 8, and 12, respectively, including the bridge (i.e., Bridge 410 of Fig. 4) is performing as the terminating point (i.e., ending connection point between PCI protocol and I/O Links; See Figs. 2, 4, and 5) for data signals received from the network (i.e., I/O Links 112 in Fig. 1) through the switch (i.e., Crossbar Switch & Arbiter 408 of Fig. 4; See col. 5, lines 52-55), except that does not expressly teach said bridge comprising an edge node.

Ravinovitz discloses a StarFabric implementation (See paragraph [0060]), wherein

- a bridge (i.e., StarGen SG2010 bridge chip; See paragraph [0061]) comprising an edge node that is a terminating point for data signals received (See paragraph [0069], lines 1-6) from a network through a switch (See paragraph [0068]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said StarFabric implementation, as disclosed by Ravinovitz, in said bridge (i.e., Bridge), as disclosed by Chan, for the advantage of providing root node and leaf node features, wherein said root node supports an initiation of network resets (i.e., fabric resets) and enumeration (See Ravinovitz, paragraph [0069], lines 6-8).

11. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan [US 6,950,893 B2] as applied to claims 1-3, 5-7, and 9-11 above, and further in view of Craddock et al. [US 2003/0050990 A1; hereinafter Craddock].

Referring to claim 13, Chan discloses all the limitations of the claim 13, except that does not teach that a data bus space on the data bus of a first circuit card of the plurality of circuit

cards on the network comprises an address range with blocks that are mapped to the processor on a second circuit card of the plurality of circuit cards on the network.

Craddock discloses a mechanism for initiating and completing one or more I/O transactions using memory semantic messages in a system area network (See Abstract),

- a data bus space (i.e., virtually contiguous memory space) on a data bus (i.e., bus system 134 of Fig. 1) of a first circuit card (e.g., Host Processor node 102 of Fig. 1) of a plurality of circuit cards (i.e., Host Processor nodes 102, 104 in Fig. 1) on a network (i.e., SAN Fabric 116 in Fig. 1; See paragraph [0045]) comprising an address range with blocks (i.e., a portion of a memory region or a portion of a memory window) that are mapped to a processor (i.e., CPUs 136-140 in Fig. 1) on a second circuit card (e.g., Host Processor node 104 of Fig. 1) of the plurality of circuit cards on the network (i.e., said Host Processor nodes on said SAN Fabric; See paragraph [0062]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said mechanism for initiating and completing one or more I/O transactions using memory semantic messages, as disclosed by Craddock, in said system (i.e., computer system), as disclosed by Chan, for the advantage of providing said mechanism using memory semantic messages so as to allow easy migration of Peripheral Component Interconnect (PCI) devices (See Craddock, paragraph [0009], lines 16-22).

Referring to claim 14, Craddock teaches

- when the processor of the first circuit (i.e., CPUs 126-130 on Host Processor node 102 of Fig. 1) reads or writes into the data bus space (i.e., virtually contiguous memory space), data is routed over the network (i.e., SAN Fabric 116 in Fig. 1) to the processor

on the second circuit card (i.e., CPUs 136-140 on Host Processor node 104 of Fig. 1; See paragraph [0063] for read operation, and paragraph [0064] for write operation).

Response to Arguments

12. Applicants' arguments with respect to the amended claims 1 and 2, and furthermore, the newly added claim 6, have been considered but are moot in view of the new ground(s) of rejection.

Actually, the Examiner brought Chan, Ravinovitz, and Craddock references in the rejection for the limitations which are not provided by Chakrabarti and all of the other art cited[*].

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Brocco et al. [US 6,996,658 B2] disclose multi-port system and method for routing a data element within an interconnection fabric.

Heil [US 6,944,152 B1] discloses data storage access through switched fabric.

Chan [US 2004/0059862 A1] discloses method and apparatus for providing redundant bus control.

Jones [US 6,882,645 B2] discloses apparatus and method for sequencing memory operations in an asynchronous switch fabric.

Olarig et al. [US 2003/0126297 A1] disclose network processor interface system.

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[*] See paragraph 7 of the instant Office Action, Claims 1-3, 5-7, and 9-11 rejection under 35 U.S.C. 102(e) as being anticipated by Chan.
See paragraph 10 of the instant Office Action, Claims 4, 8, and 12 rejection under 35 U.S.C. 103(a) as being unpatentable over Chan in view of Ravinovitz.
See paragraph 11 of the instant Office Action, Claims 13 and 14 rejection under 35 U.S.C. 103(a) as being unpatentable over Chan in view of Craddock.

Bunton [US 7,010,607 B1] discloses method for training a communication link between ports to correct for errors.

Harris et al. [US 2003/0235042 A1] disclose carrier card and method.

Harris et al. [US 2004/0003154 A1] disclose computer system and method of communicating.

Scott et al. [US 7,009,982 B2] disclose combining narrowband applications with broadband transport.

Blanc et al. [US 6,667,955 B1] disclose switching fabric system having at least one subsystem including switch core elements arranged in port expansion architecture.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Patent Examiner
Art Unit 2112

CEL/